Application No.: 10/715,931 Docket No.: 386998039US

AMENDMENTS TO THE CLAIMS

53. (previously presented) A nonvolatile memory with undercut trapping structure, said nonvolatile memory comprising:

a semiconductor substrate;

a gate oxide formed on said semiconductor substrate;

a gate structure formed on said gate oxide, wherein said gate structure including a undercut structure formed at lower portion of the gate structure and inwardly into said gate structure;

an isolation layer formed over the sidewall of said gate structure;

first spacers formed on the sidewall of said isolation layer and filled into said undercut structure for storing carriers;

source and drain regions formed adjacent to said gate structure and under said undercut structure; and

double doped drain region adjacent to said source and drain regions and under said undercut structure, wherein the junction of said double doped drain region is deeper than the one of said source and drain regions and said double doped drain region is closer to the channel under said gate structure than said source and drain regions; and

pocket ion implantation region located adjacent to said source and drain regions and under said undercut structure, wherein the conductive type of the pocket ion implantation region is opposite to the one of the source and drain regions.

54. (previously presented) The nonvolatile memory of Claim 53, wherein the undercut-filling material filled into said undercut structure includes nitride or the material having energy gap lower than 6eV, said first spacers attached onto the sidewall of said gate is formed of oxide or the material having energy gap larger than 7eV.

55. (previously presented) The nonvolatile memory of Claim 53, further comprising second spacers attached on said first spacers, wherein said second spacers is formed of oxide or the material having energy gap larger than 7eV.

56. (previously presented) A nonvolatile memory with undercut trapping structure, said nonvolatile memory comprising:

a semiconductor substrate;

a gate oxide formed on said semiconductor substrate;

a gate structure formed on said gate oxide, wherein said gate structure including a undercut structure formed at lower portion of the gate structure and inwardly into said gate structure;

an isolation layer formed over the sidewall of said gate structure;

first spacers formed on the sidewall of said isolation layer and filled into said undercut structure for storing carriers;

source and drain regions formed adjacent to said gate structure and under said undercut structure; and

pocket ion implantation region adjacent to said double doped drain region and under said undercut structure, wherein the conductive type of the pocket ion implantation region is opposite to the one of the source and drain regions, wherein the undercut-filling material filled into said undercut structure includes nitride or the material having energy gap lower than 6eV, said first spacers attached onto the sidewall of said gate is formed of oxide or the material having energy gap larger than 7eV.

57. (previously presented) The nonvolatile memory of Claim 56, further comprising second spacers attached on said first spacers, wherein said second spacers are formed of oxide or the material having energy gap larger than 7eV.

58. (previously presented) A nonvolatile memory with undercut trapping structure, said nonvolatile memory comprising:

a semiconductor substrate;

a gate oxide formed on said semiconductor substrate;

a gate structure formed on said gate oxide, wherein said gate structure including a undercut structure formed at lower portion of the gate structure and inwardly into said gate structure;

an isolation layer formed over the sidewall of said gate structure;

first spacers formed on the sidewall of said isolation layer and filled into said undercut structure for storing carriers;

source and drain regions formed adjacent to said gate structure and under said undercut structure; and

lightly doped drain region adjacent to said source and drain regions and under said undercut structure, wherein the junction of said lightly doped drain region is shallower than the one of said source and drain regions and said lightly doped drain region is closer to the channel under said gate structure than said source and drain regions; and

pocket ion implantation region located adjacent to said source and drain regions and under said undercut structure, wherein the conductive type of the pocket ion implantation region is opposite to the one of the source and drain regions, wherein the undercut-filling material filled into said undercut structure includes nitride or the material having energy gap lower than 6eV, said first spacers attached onto the sidewall of said gate is formed of oxide or the material having energy gap larger than 7eV.

59. (previously presented) The nonvolatile memory of Claim 58, further comprising second spacers attached on said first spacers, wherein said second spacers is formed of oxide or the material having energy gap larger than 7eV.

60. (previously presented) A nonvolatile memory with undercut trapping structure, said nonvolatile memory comprising:

a semiconductor substrate;

a gate oxide formed on said semiconductor substrate;

a gate structure formed on said gate oxide, wherein said gate structure including a undercut structure formed at lower portion of the gate structure and inwardly into said gate structure, wherein said gate structure comprising a stacked structure including of polysilsicon layer/silicide layer and a first dielectric layer;

a second dielectric layer formed over the sidewall of said gate structure;

first spacers formed on the sidewall of said second dielectric layer and filled into said undercut structure for storing carriers; and

source and drain regions formed adjacent to said gate structure and under said undercut structure; and

pocket ion implantation region located adjacent to said source and drain regions and under said undercut structure, wherein the conductive type of the pocket ion implantation region is opposite to the one of the source and drain regions, wherein the undercut-filling material filled into said undercut structure includes nitride or the material having energy gap lower than 6eV, said first spacers attached onto the sidewall of said gate is formed of oxide or the material having energy gap larger than 7eV.

61. (previously presented) The nonvolatile memory of Claim 60, further comprising second spacers attached on said first spacers, wherein said second spacers is formed of oxide or the material having energy gap larger than 7eV.

62. (previously presented) A nonvolatile memory with undercut trapping structure, said nonvolatile memory comprising:

a semiconductor substrate;

a gate oxide formed on said semiconductor substrate;

a gate structure formed on said gate oxide, wherein said gate structure including a undercut structure formed at lower portion of the gate structure and inwardly into said gate structure, wherein said gate structure comprising a stacked structure including of polysilsicon layer/silicide layer and a first dielectric layer;

a second dielectric layer formed over the sidewall of said gate structure;

first spacers formed on the sidewall of said second dielectric layer and filled into said undercut structure for storing carriers; and

source and drain regions formed adjacent to said gate structure and under said undercut structure;

lightly doped drain region adjacent to said source and drain regions and under said undercut structure, wherein the junction of said lightly doped drain region is shallower than the one of said source and drain regions and said lightly doped drain region is closer to the channel under said gate structure than said source and drain regions; and

pocket ion implantation region adjacent to said lightly doped drain regions, wherein the conductive type of the pocket ion implantation region is opposite to the one of the source and drain regions, wherein the undercut-filling material filled into said undercut structure includes nitride or the material having energy gap lower than 6eV, said first spacers attached onto the sidewall of

said gate is formed of oxide or the material having energy gap larger than 7eV.

63. (previously presented) The nonvolatile memory of Claim 62, further comprising second spacers attached on said first spacers, wherein said second spacers is formed of oxide or the material having energy gap larger than 7eV.

64. (previously presented) A nonvolatile memory with undercut trapping structure, said nonvolatile memory comprising:

a semiconductor substrate;

a gate oxide formed on said semiconductor substrate;

a gate structure formed on said gate oxide, wherein said gate structure including a undercut structure formed at lower portion of the gate structure and inwardly into said gate structure, wherein said gate structure comprising a stacked structure including of polysilsicon layer/silicide layer and a first dielectric layer;

a second dielectric layer formed over the sidewall of said gate structure;

first spacers formed on the sidewall of said second dielectric layer and filled into said undercut structure for storing carriers; and

source and drain regions formed adjacent to said gate structure and under said undercut structure;

double doped drain region adjacent to said source and drain regions and under said undercut structure, wherein the junction of said double doped drain region is deeper than the one of said source and drain regions and said double doped drain region is closer to the channel under said gate structure than said source and drain regions; and

pocket ion implantation region adjacent to said double doped drain regions, wherein the conductive type of the pocket ion implantation region is opposite to the one of the source and drain regions, wherein the undercut-filling material

filled into said undercut structure includes nitride or the material having energy gap lower than 6eV, said first spacers attached onto the sidewall of said gate is formed of oxide or the material having energy gap larger than 7eV.

65. (previously presented) The nonvolatile memory of Claim 64, further comprising second spacers attached on said first spacers, wherein said second spacers is formed of oxide or the material having energy gap larger than 7eV.

66. (currently amended) A nonvolatile memory with undercut trapping structure, said nonvolatile memory comprising:

a semiconductor substrate;

a gate oxide formed on said semiconductor substrate;

a gate structure formed on said gate oxide, wherein said gate structure including a undercut structure formed at lower portion of the gate structure and inwardly into said gate structure;

an isolation layer formed over the sidewall of said gate structure;

first spacers formed on the sidewall of said isolation layer and filled into said undercut structure for storing carriers;

source and drain regions formed adjacent to said gate structure and under said undercut structure; ~~and~~

wherein the undercut-filling material filled into said undercut structure includes nitride or the material having energy gap lower than 6eV, said first spacers attached onto the sidewall of said gate is formed of oxide or the material having energy gap larger than 7eV; and

further comprising a double doped drain region adjacent to said source and drain regions and under said undercut structure, wherein the junction of said double doped drain region is deeper than the one of said source and drain

regions and said double doped drain region is closer to the channel under said gate structure than said source and drain regions. .

67. (cancelled) The nonvolatile memory of Claim 66, further comprising double doped drain region adjacent to said source and drain regions and under said undercut structure, wherein the junction of said double doped drain region is deeper than the one of said source and drain regions and said double doped drain region is closer to the channel under said gate structure than said source and drain regions.

68. (currently amended) The nonvolatile memory of Claim 6~~7~~6, further comprising pocket ion implantation region adjacent to said double doped drain region and under said undercut structure, wherein the conductive type of the pocket ion implantation region is opposite to the one of the source and drain regions.

69. (previously presented) The nonvolatile memory of Claim 66, further comprising lightly doped drain region adjacent to said source and drain regions and under said undercut structure, wherein the junction of said lightly doped drain region is shallower than the one of said source and drain regions and said lightly doped drain region is closer to the channel under said gate structure than said source and drain regions.

70. (previously presented) The nonvolatile memory of Claim 66, further comprising second spacers attached on said first spacers, wherein said second spacers are formed of oxide or the material having energy gap larger than 7eV.

71. (currently amended) A nonvolatile memory with undercut trapping structure, said nonvolatile memory comprising:

a semiconductor substrate;

a gate oxide formed on said semiconductor substrate;

a gate structure formed on said gate oxide, wherein said gate structure including a undercut structure formed at lower portion of the gate structure and inwardly into said gate structure, wherein said gate structure comprising a stacked structure including of polysilsicon layer/silicide layer and a first dielectric layer;

a second dielectric layer formed over the sidewall of said gate structure;

first spacers formed on the sidewall of said second dielectric layer and filled into said undercut structure for storing carriers; and

source and drain regions formed adjacent to said gate structure and under said undercut structure; ~~and~~

wherein the undercut-filling material filled into said undercut structure includes nitride or the material having energy gap lower than 6eV, said first spacers attached onto the sidewall of said gate is formed of oxide or the material having energy gap larger than 7eV; and

further comprising a double doped drain region adjacent to said source and drain regions and under said undercut structure, wherein the junction of said double doped drain region is deeper than the one of said source and drain regions and said double doped drain region is closer to the channel under said gate structure than said source and drain regions..

72. (cancelled) The nonvolatile memory of Claim 71, further comprising double doped drain region adjacent to said source and drain regions and under said undercut structure, wherein the junction of said double doped drain region is deeper than the one of said source and drain regions and said double doped drain region is closer to the channel under said gate structure than said source and drain regions.

73. (currently amended) The nonvolatile memory of Claim 71~~2~~, further comprising pocket ion implantation region adjacent to said double doped drain region and

under said undercut structure, wherein the conductive type of the pocket ion implantation region is opposite to the one of the source and drain regions.

74. (previously presented) The nonvolatile memory of Claim 71, further comprising lightly doped drain region adjacent to said source and drain regions and under said undercut structure, wherein the junction of said lightly doped drain region is shallower than the one of said source and drain regions and said lightly doped drain region is closer to the channel under said gate structure than said source and drain regions.

75. (previously presented) The nonvolatile memory of Claim 71, further comprising second spacers attached on said first spacers, wherein said second spacers are formed of oxide or the material having energy gap larger than 7eV.

76. (previously presented) A nonvolatile memory with undercut trapping structure, said nonvolatile memory comprising:

a semiconductor substrate;

a gate oxide formed on said semiconductor substrate;

a gate structure formed on said gate oxide, wherein said gate structure including a undercut structure formed at lower portion of the gate structure and inwardly into said gate structure;

an isolation layer formed over the sidewall of said gate structure;

first spacers formed on the sidewall of said isolation layer and filled into said undercut structure for storing carriers;

source and drain regions formed adjacent to said gate structure and under said undercut structure;

salicide formed on said gate structure and said source and drain regions;

double doped drain region adjacent to said source and drain regions and under said undercut structure, wherein the junction of said double doped drain region is deeper than the one of said source and drain regions and said double doped

drain region is closer to the channel under said gate structure than said source and drain regions; and

pocket ion implantation region located adjacent to said source and drain regions and under said undercut structure, wherein the conductive type of the pocket ion implantation region is opposite to the one of the source and drain regions; wherein said isolation layer is formed of oxide or the material having energy gap larger than 7 eV.

77. (previously presented) The nonvolatile memory of Claim 76, wherein said first spacers are formed of nitride or the material having energy gap lower than 6eV.

78. (previously presented) The nonvolatile memory of Claim 76, wherein said silicide material includes $TiSi_2$, $CoSi_2$ or NiSi.

79. (previously presented) A nonvolatile memory with spacer trapping structure, said nonvolatile memory comprising:

a semiconductor substrate;

a gate oxide formed on said semiconductor substrate;

a gate structure formed on said gate oxide, wherein said gate structure comprises a stacked structure including of polysilsicon layer/silicide layer and a first dielectric layer;

a second dielectric layer formed on the sidewall of said gate structure and the surface of said semiconductor substrate;

first spacers formed on the sidewall of said second dielectric layer;

source and drain regions formed adjacent to said gate structure, wherein p-n junctions of said source and drain regions formed under said first spacers;

double doped drain region adjacent to said source and drain regions, wherein the p-n junctions of said double doped drain region are formed under said first spacers and the junction of said double doped drain region being deeper

than the one of said source and drain regions, said double doped drain region being closer to the channel under said gate structure than said source and drain regions and the doping concentration of said double doped drain region is lower than the one of said source and drain regions;

pocket ion implantation region adjacent to said double doped drain region, the conductive type of the pocket ion implantation region being opposite to the one of the source and drain regions; and

wherein said wherein said second dielectric layer is formed of oxide or the material having energy gap larger than 7eV.

80. (previously presented) The nonvolatile memory of Claim 79, wherein said first spacers are formed of nitride or the material having energy gap lower than 6eV.

81. (previously presented) The nonvolatile memory of Claim 79, wherein said silicide material includes TiSi2, WSi2, CoSi2 or NiSi.

82. (previously presented) The nonvolatile memory of Claim 79, wherein said first dielectric layer is formed of oxide, nitride or the combination of oxide and nitride layers.